A 640x480 Resolution 326,000fps Continuous-Mode Ultra-High Speed Global-Shutter CMOS BSI Imager with Exceptional Light Sensitivity

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***Abstract*— This paper presents an ultra-high speed monolithic global-shutter CMOS image sensor offering motion capture at 326,000 FPS in continuous-mode operation with 640x480 pixel resolution. The high speed is achieved by a combination of pixel technology and circuit techniques. The highly sensitive pixel has 52µm pitch and consists of a fully depleted substrate for fast photocarrier transport. The in-pixel circuitry includes analog storage for pipelined readout and analog CDS for fast readout and low noise. The sensor achieves an equivalent row time of 6.4ns by having separate top and bottom readout with multiple parallel ADCs per column. Separate row drivers on the left and the right guarantee the global shutter accuracy required by the minimum exposure time of 59ns. The dynamic range is optimized by on-chip reduction of the FPN and by lossless data compression. The sensor throughput is as high as 100 Gpix/sec and is delivered off-chip via 128 CML channels running at 6.6 Gbps each. The sensor is fabricated in 130nm monolithic CIS process with BSI postprocessing and is currently in series production.**

I. Introduction

Ultra high-speed (UHS) global shutter image sensors are indispensable for realizing camera products capable of capturing very fast transient events. The UHS imagers fall into two broad categories, namely, burst imagers and continuous recording imagers, each catering to different application niches.

Burst imagers deploy in-pixel analog storage thereby eliminating the need to read out the pixel array after every sensor exposure. This allows capturing a short burst of frames at extremely high rates. Continuous recording imagers, on the other hand, have their pixel throughput limited by the sensor readout speed and output bandwidth. This introduces a fundamental trade-off between spatial resolution and temporal resolution offered by such imagers. A plot of spatial resolution versus frame rate (**Fig. 1**) captures the performance evolution of high-speed imagers from the published literature, both commercial and scientific. It shows significant advancements in the performance of CMOS imagers with continuous recording being offered at frame rates that easily exceed tens of thousands of FPS. As per the plot, the boundary between continuous and burst imagers occurs at the pixel rate of 100 Gpix/s and the sensor reported in this paper finds itself at the forefront of the current offerings in continuous high-speed imaging. With a novel combination of advanced pixel technology and circuit techniques, this sensor offers a throughput and sensitivity performance that exceeds the state of the art of continuous recording imagers.

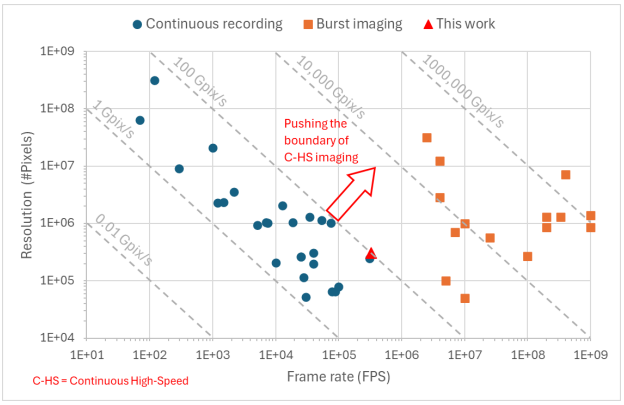

Fig. 1. High-speed imagers state-of-the-art

II. Imager Architecture

A. Pixel array

The sensor uses pixel technology and in-pixel circuit techniques specifically developed for high-speed operation [1]. The pixel diode cross section is shown in **Fig. 2**. The pixel is backside illuminated (BSI) with anti-reflective coating (ARC) and consists of a fully depleted substrate. While BSI and ARC lead to high fill-factor and quantum efficiency, the large electric field in the substrate allows for fast collection of photocarriers while minimizing pixel-to-pixel crosstalk. This results in a highly sensitive pixel. To boost the frame rate, the pixel incorporates two circuit techniques, namely, in-pixel storage for pipelined readout and in-pixel CDS for kT/C noise suppression with minimal speed loss.

Realizing an electronic global shutter requires in-pixel storage to hold the image frame while it is read out. With extra storage, the pixel can hold multiple frames, thus allowing pipelining of integration and readout to achieve higher throughput. With the same goal, this sensor uses an implementation of dual in-pixel storage earlier reported in [2] allowing integration of the new frame and readout of the previous frame to happen in parallel. A simplified schematic and timing diagram of the pixel circuit are illustrated in **Fig. 3**.

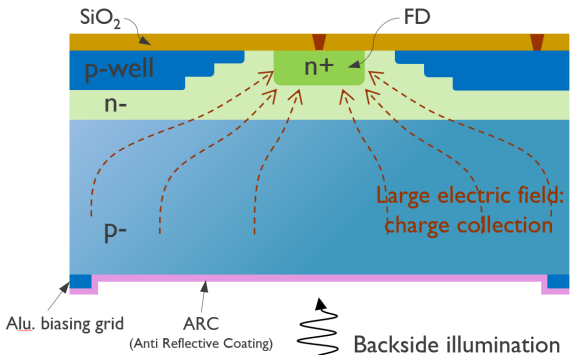

Fig. 2. Pixel diode design

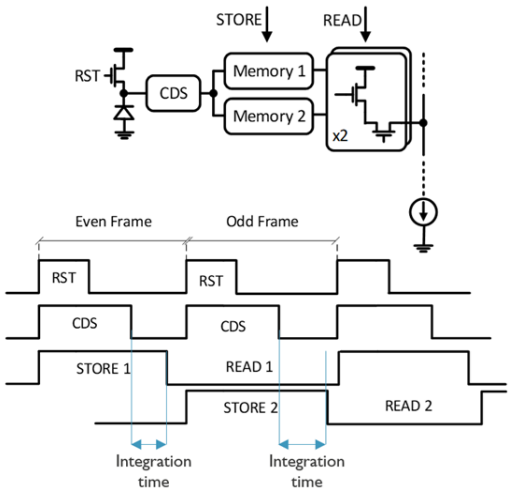

Fig. 3. Pixel circuit design (top) and timing diagram (bottom)

Low temporal noise is critical for ensuring sufficient signal sensitivity especially in imagers with exposure times as short as 59ns (this work). CMOS imagers commonly rely on digital CDS for pixel kT/C noise suppression which requires two readouts per pixel. The in-pixel CDS [3, 4] allows this sensor to perform analog CDS within single readout, thus relaxing noise-speed tradeoff. Since, the in-pixel CDS does not remove the FPN due to column line IR drop, the sensor also incorporates a mechanism to compensate this FPN [5]. As depicted in **Fig. 4**, a voltage reference equal to the column IR drop is provided to each pixel via a dummy column having identical routing and bias current as the signal column. The bottom plate of the in-pixel sampling capacitor is connected to the pixel ground during sampling and it is switched to the dummy column during readout. This effectively removes column IR drop from the signal at the end of the column.

B. Sensor architecture

The challenge of achieving very high frame rates with the large pixel array dimensions (3.3cm x 2.5cm in this work) is addressed by extensive parallelization of the column readout [6, 7]. The sensor described here deploys separate top and bottom readout with 8 ADCs within a single pixel pitch (52µm) that simultaneously convert blocks of 8 rows within the column (**Fig. 5**). With a total of 10,240 ADCs on-chip, this brings 16x relaxation in the row readout time.

To meet the global shutter accuracy target set by the minimum exposure time, separate row drivers are added to the left and to the right of the array [6, 7]. This essentially results in four independent quadrants working in parallel as shown in **Fig. 5**.

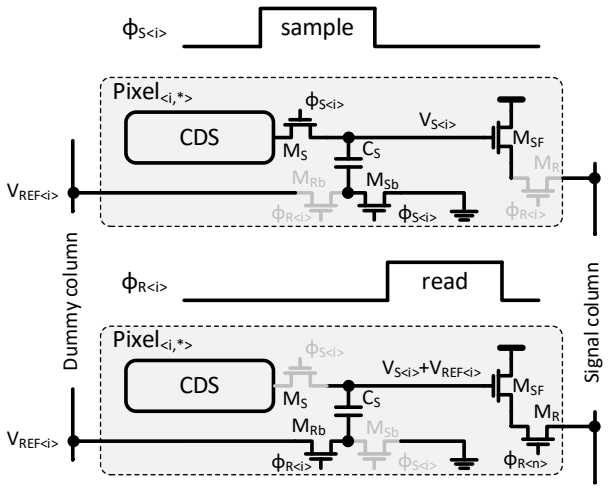

Fig. 4. Concept of vertical gradient compensation

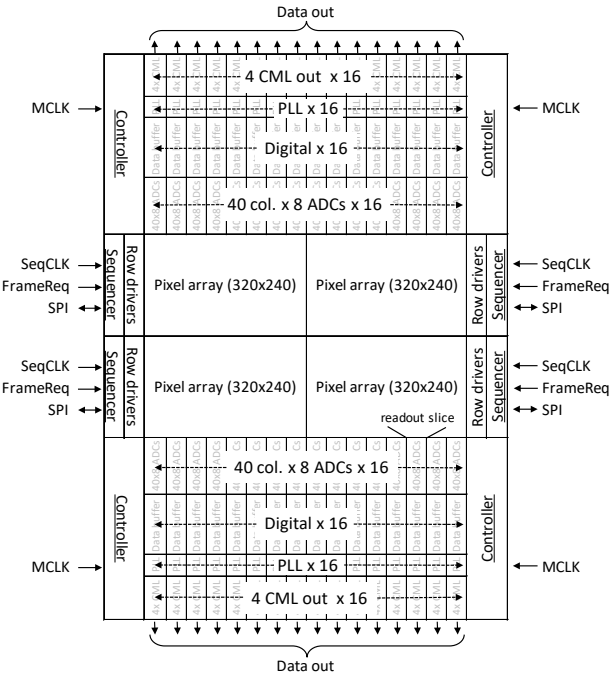

Fig. 5. Top level architecture

The readout is organized in slices mapping to 40 columns. **Fig. 6** shows block diagram of one slice which consists of 320 A/D converters followed by digital logic to perform data compression and encoding for serial transmission via 4 high-speed CML channels. The ADC is a low power asynchronous SAR that achieves 9-bit resolution at 15 MSPS throughput consuming 500µW. A PLL per slice generates 6.6GHz clock for the 4 serializers.

To reduce the data transfer rate, the 9-bit outputs of the ADCs are compressed into 8-bit words exploiting the shot noise limited SNR of the imagers at high signal levels [8]. **Fig. 7** shows the transfer characteristics of the digital encoder. The signal range is split in 3 regions. Starting at 9-bits in the lowest signal range, the number of bits is reduced by 1 for each of the subsequent signal ranges causing the RMS quantization noise to increase by 2x and 4x in those ranges. However, since the quantization noise

remains well below photon shot noise over the entire signal range, practically lossless data compression is achieved. Output data of multiple ADCs are interleaved in continuous serial bit streams which are converted to 64B/66B Xilinx Aurora protocol frames and transmitted over 6.6 Gbit/s CML outputs. The sensor packs in total 128 of these CML outputs.

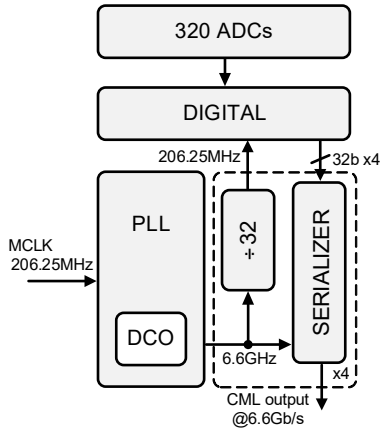

Fig. 6. Single readout slice

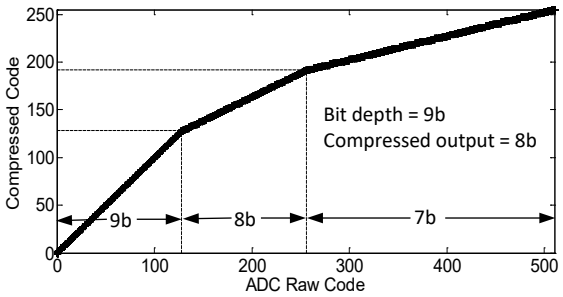

Fig. 7. Non-uniform quantization: ADC data compression

As the overall chip size is larger than the reticle size, the chip is fabricated by stitching together smaller blocks that fit within the reticle.

III. Measurement Results

The sensor described here has been silicon verified and is in series production. **Fig. 8** shows the packaged sensor mounted on a PCB that is designed to be used in the camera as well as on the testbench.

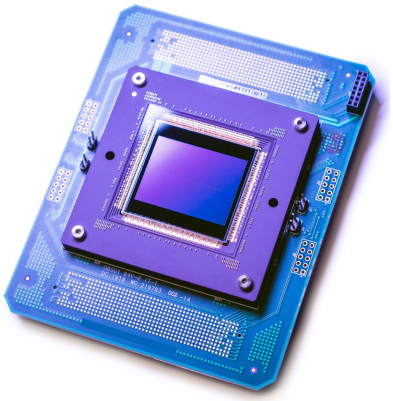

Fig. 8. Packaged BSI sensor

The sensor has been characterized using a uniform monochromatic light source. **Fig. 9** shows PTC plot of the sensor and the extraction of imager metrics, namely, conversion gain, noise floor and full well capacity. The histogram of temporal readout noise is shown in **Fig. 10**. It can be seen that 99.2% of the pixels have noise within four sigma. The results of quantum efficiency (QE) measurement are plotted in **Fig. 11**. By virtue of BSI, the sensor evidently achieves high QE.

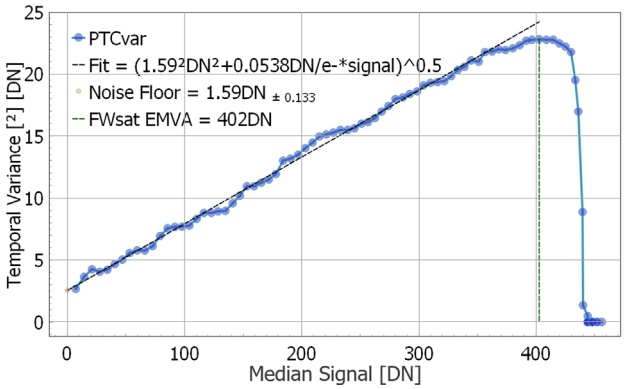

Fig. 9. Photon Transfer Curve (PTC) measurement

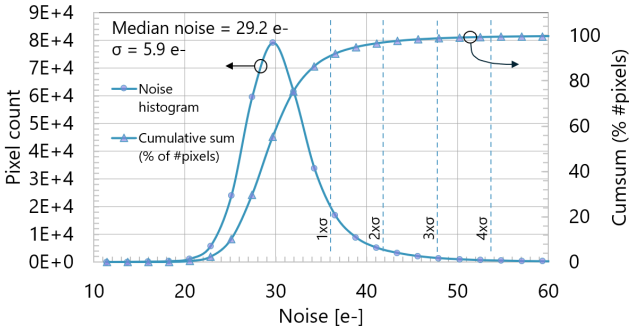

Fig. 10. Temporal readout noise histogram

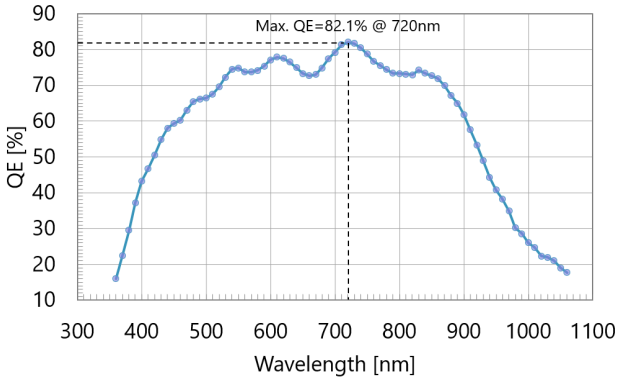

Fig. 11. Monochromatic quantum efficiency plot

Key performance specifications of the sensor are listed in **Table 1**. With EMVA 1288 absolute sensitivity threshold of 0.011 e-/µm2 and the frame rate of 326,000fps, the sensor advances the state of the art [6, 9] in respect of these metrics.

A sequence of non-successive frames captured with the imager at 240,000 FPS demonstrates the imager performance (**Fig. 12**).

IV. Conclusion

A 640x480 pixel resolution monolithic ultra high-speed, high-sensitivity continuous recording global shutter image sensor fabricated in 130nm CMOS BSI process was demonstrated. In terms of sensitivity and throughput, the sensor performance exceeds the state of the art in continuous recording high-speed imagers making it one of the fastest in this category. Low input referred noise together with fully depleted substrate and BSI post-processing enable the sensor to attain high signal sensitivity.

The sensor thus described is the beating heart of a range of high-speed camera products today on the market, enabling a host of scientific high-speed imaging applications.

Table 1

Performance Comparison

Parameter	This work	[6]	[9]
Technology	130 nm, 5 metal CMOS, BSI	110 nm, 6 metal CMOS, BSI	CMOS, BSI
Binning	Not available	2 x 2	2 x 2
Resolution	640 x 480	1280 x 832	Binned 640x384
Pixel pitch	52 µm	18.54 µm	Binned 37 µm
Shutter type	Global	Global	Global
FWC	7.5 ke-	N/A	33 ke-
Conversion gain	0.054 DN/e-	N/A	N/A
QE @ 532 nm	72.7%	N/A	72.0%
Max. FPS (max. ROI)	326,000	80,000	308,820
Equivalent row time	6.4 ns	15.0 ns (no binning)	8.4 ns
Readout noise	29.5 e- RMS	N/A	70.7 e- RMS

Parameter	This work	[6]	[9]
$\mu_{e.min.area}$‡ (EMVA 1288)	0.011 e-/µm^2	N/A	0.056 e-/µm^2†
Min. integration time	59 ns	Binned 95 ns	95 ns / 38 ns
Dynamic range	48 dB	52 dB	53.4 dB
Bit depth	9 bits	10/11/12 bits depending on row time	12 bits
Output channels	128 channels @ 6.6 Gbps	160 channels @ 6.25 Gbps	N/A
Image lag	1 DN (9-bit)	N/A	N/A
Non-linearity	< 5%	< 1.75%	1.29%†
Dark current @ room temperature	3.41 nA/cm^2	N/A	2.3 nA/cm^2†
Power consumption	25 W	< 40 W	N/A

† Extracted from EMVA 1288 report for binned mode ‡ Absolute sensitivity threshold (QE not included)

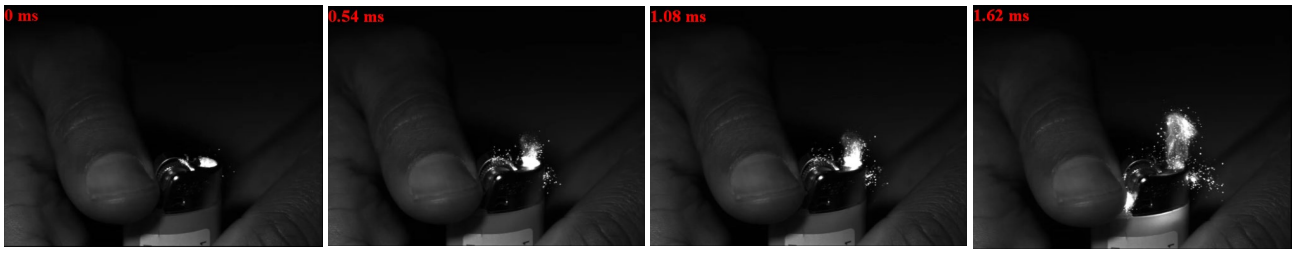

Fig. 12. Four non-successive 640x480 frames from a 240,000 fps video of lighter ignition at 2 µs exposure

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